IN THE ABSTRACT:

Please delete the existing Abstract and replace it in its entirety with the following:

--A method of generating synthesis scripts to synthesize integrated circuit (IC) designs described in a generic netlist into a gate-level description includes the steps of identifying hardware elements in a generic netlist, determining key pins for each of the identified hardware elements, extracting design structure and hierarchy from the generic netlist, generating script to cause a logic synthesis tool to apply bottom-up synthesis to modules and sub-modules of the IC design, generating script to cause a logic synthesis tool to apply top-down characterization to modules and sub-modules of the IC design, and generating script to cause a logic synthesis tool to repeat these bottom-up and top-down applications until constraints are satisfied.--

## REMARKS

Claims 1 to 6 and 9 to 20 are now pending in the application, with claims 1, 9, 10, 11, 13 and 14 being the independent claims. Reconsideration and further examination are respectfully requested.

In the Office Action, objection was made to the Abstract. Accordingly, the Abstract has been rewritten as set forth above. Withdrawal of this objection is therefore respectfully requested.

Objection also was made to the disclosure based on certain alleged informalities. In response, Applicant has amended the specification as set forth above. However, with respect to the correction requested at lines 5 and 25 of page 16 of the specification, it is believed that "multiply-driven" is grammatically correct. Specifically, because "driven" is an adjective, it must be modified by an adverb, such as "multiply", rather than another adjective, such as "multiple". Based on the above amendments to the specification and the foregoing remarks, withdrawal of this objection is respectfully requested.

Claims 1 to 14 were rejected under 35 U.S.C. §102(e) over U.S. Patent 5,812,416 (Gupte); and claim 7 was also rejected under 35 U.S.C. §103(a) over Gupte. The above cancellation of claims 7 and 8 has rendered the rejection of those claims moot. Withdrawal of the § 102 rejections is respectfully requested for the following reasons.

Independent claims 1, 11 and 13 are directed to generation of synthesis scripts to synthesize integrated circuit (IC) designs in RTL level description into gate-level description. Hardware elements are identified in the generic netlist and key pins are determined for each of the identified hardware elements. Critical design structure and hierarchy are extracted from the generic netlist. Bottom-up synthesis is applied to modules and sub-modules of the IC design. Top-down characterization is applied to modules and sub-modules of the IC design, with such bottom-up and top-down applications being repeated until constraints are satisfied.

The forgoing combination of features is not disclosed or suggested by the applied art. In particular, the applied art does not disclose or to suggest at least the features of: (1) identifying hardware elements in a generic netlist and key pins for each of the identified hardware elements; and (2) repeating bottom-up synthesis and top-down characterization until constraints are satisfied.

In this regard, it is asserted in the Office Action that Gupte's step of processing HDL code, described at column 14, lines 12 to 17, inherently involves identifying hardware elements in a generic netlist and determining key pins for each of the identified hardware elements. In response, it is noted that HDL code is significantly different than a generic netlist. Specifically, although a generic netlist often is created based on HDL code, both the type and format of the data provided in these two different descriptions are significantly different. Accordingly, it is not believed that parsing HDL code can be said to inherently involved identifying hardware elements in a generic netlist and determining key pins for the identified hardware elements. In particular, although pins ordinarily are defined in a generic netlist, no identification of pins is typically present in HDL. Therefore, not only would identification of pins not be inherently involved in parsing HDL code, but, in fact, identifying pins in HDL code would likely be extremely difficult.

Moreover, in the Office Action it is noted that Figure 14 indicates that top-down and bottom-up synthesis processes may be repeated. However, this is not beleived to be equivalent to repeating bottom-up synthesis and top-down characterization until

constraints are satisfied, as in the present invention. Rather, column 14, lines 52-55, of Gupte indicates that a user may repeat the process if desired. He then notes, "For example, the user may modify some constraints at the lower levels for the next iteration [emphasis added]."

Thus, Gupte is believed to be significantly different than the present invention as recited in independent claims 1, 11 and 13.

Independent claims 9, 10 and 14 include the features of: (1) determining key pins for identified hardware elements from a generic netlist; and (2) repeating steps of bottom-up synthesis and top-down characterization until constraints are satisfied. Accordingly, independent claims 9, 10 and 14 also are believed to be allowable over the applied art.

Newly added dependent claims 15 to 20 include the additional feature that I/O conditions and constraints of the modules of the IC design are captured during top-down characterization and are used to re-optimize the IC design during bottom-up synthesis. This additional feature is not believed to be disclosed or suggested by Gupte. Accordingly, for this additional reason, dependent claims 15 to 20 are believed to be allowable over the applied art.

The other claims in the application depend from the independent claims discussed above and are therefore believed to be allowable for the same reasons. Because each defines an additional aspect of the invention, however, the individual reconsideration of each on its own merits is respectfully requested.

In view of the foregoing remarks, the entire application is believed to be in condition for allowance, and an indication to that effect is respectfully requested.

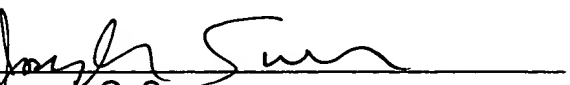
## CONCLUSION

If there are any fees due in connection with the filing of this paper that have not been accounted for in this paper or the accompanying papers, please charge the fees to our Deposit Account No. 13-3735. If an extension of time under 37 C.F.R. 1.136 is required for the filing of this paper and is not accounted for in this paper or the accompanying papers, such an extension is requested and the fee (or any underpayment thereof) should also be charged to our Deposit Account. A duplicate copy of this page is enclosed for that purpose.

Respectfully submitted,

**MITCHELL, SILBERBERG & KNUPP LLP**

Dated: January 7, 2000

By 

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